REMARKS

This paper is responsive to the Non-Final Office Action dated December 21, 2004. Claims 1-49 were examined. New claims 50-52 are added.

Status of Claims

Claims 1-52 are pending in the application. Of those, claims 1-49 currently stand rejected. All rejections are traversed. Claims 50-52 are new and recite additional dependent limitations already present in other originally presented claim sets. No new matter is added.

Drawing Objections

The Examiner objects to Fig. 1 as including a reference character (#135) not mentioned in the description. The specification has been amended to properly recite reference character 135. No new matter is added.

The Examiner objects to Fig. 3 as including several reference characters not mentioned in the description. The drawing has been amended (by Replacement Sheet) to delete the superfluous reference characters.

The Examiner objects to Fig. 6 as including a reference character (#690) not mentioned in the description. The specification has been amended to properly recite reference character 690. No new matter is added.

Claim Objections

Claim 48 is objected to for omission of punctuation (a period). The claim has been amended accordingly.

Provisional Double Patenting Rejection

Claims 1-49 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-36 of U.S. Patent No. 6,308,319 issued to Bush et al. (hereinafter "Bush 310"). Applicants respectfully defer any disclaimer (if appropriate) until after claims are indicated otherwise allowable.

Art Rejections, in General

At the outset, Applicants note several major points:

1. **Legal Standard for Obviousness**: As a threshold matter, references relied upon by the Office simply do not support a *prima facie* case of obviousness. Details are given (below) with respect to individual claims, but as a general matter the Office's approach appears to be to identify a few (though not all) items recited in a claim (e.g., an "instruction," a "safe point" or a feature that the Office interprets as an "interrupt" mechanism) in references that have nothing to do with the subject matter of Applicants' claims, hypothecate combination based on the recipe of Applicants' own disclosure and claims, and declare obviousness. In doing so, the Office commits legal error. In particular, the Office ignores many of the substantive limitations of the claim and, significantly, fails to identify any teaching, suggestion or motivation ***in the art*** to combine the disparate unrelated teachings (of the alleged "prior art') in the manner claimed.

   In this regard, Applicants respectfully traverse each obviousness rejection and requests that the Office reconsider, particularly for consistency with *In re Lee*, 277 F.3d 1338, 61 USPQ2d 1430 (Fed. Cir. 2002).

2. **Priority Date**: Applicants have properly claimed and are entitled (under 35 U.S.C. § 120) to a priority date of 22-February-1999. Even if the relied upon references supported a *prima facie* case of obviousness (which they do not), the obviousness rejections are not based on a set of references that predate 22-February-1999. Those references that do not predate Applicants' priority do not constitute prior art under any section of 35 U.S.C. §102.

   At least each of the independent claims finds support in accordance with 35 U.S.C. § 112 in the disclosure of U.S. Patent 6,308,319 to which the present application claims priority. Applicants respectfully note that neither *Rozas* nor *Charnell* antedate Applicants' priority date and cannot support an obviousness rejection of claims that find support in the '319 patent.

3. **Official Notice**: Applicants understand the potential efficiencies (for the Office) of "Official Notice" practice. However, the Office must conform its use of Official Notice with the significant limitations thereon. In general, official notice may be appropriate for facts which are "capable of such instant and unquestionable demonstration as to defy dispute." *See generally*, MPEP 2144.03 and numerous authorities cited therein.

   In the present rejection, the Office has relied on "Official Notice" on at least 18 separate occasions. In some cases, the Office employs official notice in a way whose scope is unclear (e.g., "Official Notice is taken 'encoding parallelism', mutator code', and compiler knowledge of 'safe points' to permit process interrupts are well known in the art) or as a legal conclusion (e.g., "Official Notice is taken that Kawaguchi's invention could have been modified to accommodate a JIT compiler, as they are well known in the art for receiving source code and encoding an operation (including any

tray/exception) as encountered") or as a legal interpretation of claim language (e.g., "Official Notice is given that an 'unused position in the instruction sequence' is typically a no-op instruction that allows the system a cycle to handle data.")

More formally, Applicants specifically dispute the Office's use of Official Notice in rejection of at least claims 1, 2, 3, 4, 6, 11, 15, 18, 21, 22, 23, 24, 25, 30, 32, 35, 36-41, 42, 43-45, and 47. In each case, reliance on "Official Notice" is improper and Applicants hereby demand that the Examiner produce authority for the particular factual positions asserted. Details are given below.

For each of the preceding reasons, Applicants respectfully traverse the obviousness rejections as detailed more completely below.

Art Rejection Under 35 U.S.C. §103, Kawaguchi and Rozas

Claims 1-29, 32, and 34-49 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,557,771 to Kawaguchi et al. (hereinafter *Kawaguchi*) in view of U.S. Patent No. 6,738,893 to Rozas (hereinafter *Rozas*). Applicants respectfully ***traverse***.

Claims 1-14

Turning first to claim 1, and as best as can be understood, the Office appears to reject based on the theory that (1) safe points must be inherent in any executable code and will inevitably coincide with an instruction that may include multiple component operations if the executable code is compiled for a processor that implements such an instruction set and that (2) *Kawaguchi* discloses a suspension mechanism. The Office relies on *Rozas* for teaching one instruction set that includes multiple component operations, namely a VLIW instruction set. Without conceding point (1), Applicants respectfully note that neither *Kawaguchi* nor *Rozas* disclose or suggest code that uses one of the component operations of an instruction to selectively trigger, based on a settable state of a processor, suspension of mutator code at a safe point that coincides with the instruction. Claim 1 is allowable for at least this reason.

Kawaguchi discloses a data protection mechanism in which auxiliary bits are provided in association with addressable storage locations in memory. Based on the state of such an auxiliary bit, a read or write access directed to the associated storage location may be interrupted and an interrupt service process may be invoked to provide appropriate data protection checks

(e.g., user privilege to access the location) or allow the access to complete. With all due respect, *Kawaguchi* does not disclose or suggest placement of any thread suspension triggering operation in a code sequence to coincide with a safe point in that code sequence, let alone placement of any such operation as one of the component operations of a multi-operation instruction construct, where the multi-operation instruction coincides with a safe point.

For at least this reason, claim 1 and those dependent therefrom (2-14) are **allowable**.

For completeness, Applicants specifically **dispute** the Office's use of Official Notice taken with respect to "safe point," "encoding parallelism," and "mutator code." Applicants mechanism that uses an operation of an instruction construct that *encodes parallelism* and which coincides with a *safe point* in *mutator code* to selectively trigger, based on a settable state of a processor, suspension of the *mutator code* at the *safe point* is not capable of such instant and unquestionable demonstration in the art as to defy dispute. Applicants hereby **demand** that the Examiner produce authority for the particular factual positions asserted.

Claim 2

No use of a conditional trap operation as claimed has been cited by the Office and claim 2 is **allowable** at least for this reason.

The Office's reliance on Official Notice is legally improper. In essence, the Office seems to be arguing that use (as claimed) of a conditional trap operation is unquestionably in the prior art because Kawaguchi uses an interrupt in his data protection scheme. The conclusion does not follow from the premise. Applicants **dispute** and **demand** authority.

Claim 3

No use of a suspension triggering operation in an otherwise unused position of a VLIW instruction has been cited by the Office and claim 3 is **allowable** at least for this reason.

The Office's reliance on Official Notice is legally improper. In essence, the Office seems misunderstand the legal inquiry for obviousness and instead attempts to take "Official Notice" of a motivation to incorporate a VLIW instruction into *Kawaguchi*. The Office also seeks to leverage "Official Notice" as to compiler operation to suggest that purposeful placement of a

suspension triggering operation in an otherwise unused position of a VLIW instruction is unquestionably in the prior art. It is not. Applicants **dispute** and **demand** authority.

Claim 4

Nothing in the art of record discloses or suggests use of safe point coinciding instances of suspension triggering operations in each of plural threads of a mutator process where such operations are responsive to storage accessible to the multiple threads. Claim 4 is **allowable** at least for this reason.

Again, the Office's reliance on Official Notice is legally improper. In essence, the Office seems misunderstand the legal inquiry for obviousness and instead attempts to take "Official Notice" of a motivation to modify *Kawaguchi* (which does not disclose a multithreaded mechanism) to coordinate suspension of multiple concurrent threads. The Office also seeks to leverage "Official Notice" as to multithreading to suggest that definition of safe points in coordinated threads of a mutator as claimed is unquestionably in the prior art.. It is not. Again Applicants **dispute** and **demand** authority.

Claims 5-14

Claims 5-14 are allowable at least for the reasons give above with respect to claim 1.

Regarding claim 11, the Office's reliance on Official Notice is again legally improper. In essence, the Office seems to misunderstand the legal inquiry for obviousness and instead attempts to take "Official Notice" of a motivation to combine *Kawaguchi* (which has nothing at all to do with garbage collection) with garbage collector code as specifically recited in claim 11. Applicants **dispute** and **demand** authority.

Claims 15-20

Neither *Kawaguchi* nor *Rozas* disclose or suggest:

- use of an "`instance of an instruction coinciding with the safe point, wherein the instruction instance references storage encodable with an exception triggering value to trigger an exception for suspending the mutator at the safe point`" OR

- "in response to a start garbage collection event, encoding the storage with the exception triggering value, and thereafter executing the instruction instance, thereby triggering the exception; and in response to the exception, suspending the mutator at the safe point."

Accordingly, no *prima facie* case of obviousness has been made and claim 15 and those dependent therefrom (16-20) are **allowable** at least for this reason.

Furthermore, Applicants respectfully note that at least claims 15, 16, 18 and 20 find full support in U.S. Patent 6,308,319 to which the present application claims priority. The Office relies on *Rozas* (in addition to *Kawaguchi*) in its obviousness rejection. Since Applicants' priority antedates *Rozas*, no prima facie case of obviousness is made. The aforementioned claims are each **allowable** for at least this reason as well.

Still further, the Office relies on "Official Notice" for what must be the substance of the obviousness argument, i.e., that the substantial infrastructure of a thread suspending, garbage collected memory implementation is so similar *Kawaguchi's* trap on data protection bit technique as to motivate a person having ordinary skill in the art to build such a system using *Kawaguchi's* interrupt mechanism. The Office may not substitute mere Examiner assertion for specific factual findings and some concrete evidence on the record to support an obviousness rejection. *See In re Lee*, 277 F.3d at 1344-45, 61 USPQ2d at 1434-35; *In re Zurko,* 258 F.3d 1379, 1386, 59 U.S.P.Q.2d 1693, 1697 (Fed. Cir. 2001); MPEP 2144.03.

Applicants specifically **dispute** the Office's use of Official Notice taken with respect to "garbage collection." Applicants recite garbage collection mechanisms that, responsive to start event, encode storage with an exception triggering value, and employ an instance of an instruction that coincides with a safe point in mutator code to reference the storage and thereby trigger suspension of the mutator at the safe point. Such mechanisms are not capable of such instant and unquestionable demonstration in the art as to defy dispute. Applicants hereby **demand** that the Examiner produce authority for the particular factual positions asserted.

Claim 16

No reference for *encoding a safe-point-coinciding instruction in an otherwise unused instruction position* has been cited by the Office. Accordingly, there is no *prima facie* case of obviousness and claim 16 is **allowable** at least for this reason. *Rozas* does not precede Applicants' priority date. Claim 16 is allowable for this reason as well.

Claim 17

No reference for *encoding a safe-point-coinciding instruction in an otherwise unallocated position with a VLIW instruction* has been cited by the Office. Accordingly, there is no *prima facie* case of obviousness and claim 17 is **allowable** at least for this reason. To the extent that the Office relies on Official Notice (as taken in rejection of claim 3), Applicants **dispute** and **demand** authority as provided above.

Claim 18

No reference for *encoding a safe-point-coinciding instruction in a delay slot* has been cited by the Office. Accordingly, there is no prima facie case of obviousness and claim 18 is **allowable** at least for this reason. Further, the Office's reliance on Official Notice for the proposition that the delay slot of a delayed control transfer instruction is typically a NOOP instruction is nonsensical as applied to Applicants' claim. Applicants do not recite a NOOP. For completeness, Applicants **dispute** and **demand** authority for the proposition as apparently applied in the rejection of claims. Still further, *Rozas* does not precede Applicants' priority date and Claim 18 is allowable for this reason as well.

Claim 19

No reference for *encoding a safe-point-coinciding instruction in a VLIW instruction* has been cited by the Office. Accordingly, there is no prima facie case of obviousness and claim 19 is **allowable** at least for this reason. To the extent that the Office relies on Official Notice (as taken in rejection of claim 3), Applicants **dispute** and **demand** authority as provided above.

Claim 20

No reference for *encoding a safe-point-coinciding instruction in a delay slot of a branch* has been cited by the Office and claim 20 is **allowable** at least for this reason. The Office's statement the delay slot of a branch is merely an example of an unused position in a VLIW instruction is incorrect. Applicants **dispute** and **demand** authority. Finally, to the extent that the Office relies on Official Notice (as taken in rejection of claim 3), Applicants **dispute** and **demand** authority as provided above.

Claims 21-24

Neither *Kawaguchi* nor *Rozas* disclose or suggest:

- "an instruction sequence including an operation that coincides with a safe point therein, wherein the operation is encoded in an otherwise unused position in the instruction sequence" and "referenc[es] a state that selectively triggers suspension of the instruction sequence at the safe point"
- where the operation is "executable at least partially in parallel with one or more operations of the instruction sequence"

Accordingly, no *prima facie* case of obviousness has been made and claim 21 and those dependent therefrom (22-24) are **allowable** at least for this reason.

Furthermore, Applicants respectfully note that at least claims 21, 22 and 23 find full support in U.S. Patent 6,308,319 to which the present application claims priority. The Office relies on *Rozas* (in addition to *Kawaguchi*) in its obviousness rejection. Since Applicants' priority antedates *Rozas*, the aforementioned claims are each **allowable** for at least this reason as well.

Still further, the Office's reliance on Official Notice for the proposition that an unused position in the instruction sequence is typically a NOOP instruction is nonsensical as applied to Applicants' claim(s). Applicants do not recite a NOOP. For completeness, Applicants **dispute** and **demand** authority for the proposition as apparently applied in rejecting the claims.

Claims 22-24

To the extent that the Office relies on Official Notice (as taken in rejection of claim 3), Applicants **dispute** and **demand** authority as provided above.

Claims 25-31

Neither *Kawaguchi* nor *Rozas* disclose or suggest:

- encoding information accessible to a collector process to identify at least a portion of a root set of storage locations at a safe point in the execution sequence of instructions; OR

- encoding in an otherwise unused operation position of an instruction instance that coincides with the safe point, a conditional trap operation that references storage encodable with an exception triggering value to trigger an exception for suspending execution of the mutator code at the safe point.

Accordingly, no *prima facie* case of obviousness has been made and claim 25 and those dependent therefrom (26-29) are **allowable** at least for this reason.

Furthermore, Applicants respectfully note that claims 25-29 find full support in U.S. Patent 6,308,319 to which the present application claims priority. The Office relies on *Rozas* (in addition to *Kawaguchi*) in its obviousness rejection. Since Applicants' priority antedates *Rozas*, the aforementioned claims are each **allowable** for at least this reason as well.

As before, the Office's reliance on Official Notice for the proposition that an unused position in an instruction sequence is typically a NOOP instruction is nonsensical as applied to Applicants' claim(s). Applicants do not recite a NOOP. For completeness, Applicants **dispute** and **demand** authority for the proposition as apparently applied in rejecting the claims.

Claims 26 and 27

Contrary to the Office's assertion, *Kawaguchi* does not disclose any identification of a root set. Root sets are not particularly relevant to non-garbage collected memory, so (Examiner's citation of Figs. 1-7 aside) it is unclear how such disclosure could be inherent to

Kawaguchi. Absent disclosure of a root set, no prima facie case of obviousness is made. Claims 26 and 27 are allowable for at least this reason.

Claims 32 and 34

Applicants respectfully request that the Office re-read the language of claim 32 which recites:

> a compiler that generates an execution sequence of instructions including an explicit encoding of parallelism amongst component operations thereof, and which encodes in an otherwise unused component operation position an operation instance that references storage encodable with an exception triggering value to trigger an exception when the operation instance is executed as part of a mutator and to thereby suspend execution of the mutator at a safe point; and
>
> a map generator that supplies a collector process with information identifying a root set of storage locations in use by the mutator for pointer storage at the safe point, the safe point coinciding with the operation instance.

It is simply not credible for the Office to assert that *Kawaguchi* and *Rozas* disclose these limitations. Claim 32 and claim 34 (which depends therefrom) are allowable and withdrawal of the rejection is requested.

Once again, the Office's reliance on Official Notice for the proposition that an unused position in an instruction sequence is typically a NOOP instruction is nonsensical as applied to Applicants' claim(s). Applicants do not recite a NOOP. For completeness, Applicants **dispute** and **demand** authority for the proposition as apparently applied in rejecting the claims.

Claims 35-41

Neither *Kawaguchi* nor *Rozas* disclose or suggest "a method of advancing plural threads to coordination points in respective execution paths thereof". In particular, neither *Kawaguchi* nor *Rozas* disclose or suggest:

- "encoding an exception triggering value in storage referenced by respective instances of one or more operations encoded in respective otherwise unused operation positions in each of the plural threads" AND
- "for each of the plural threads, suspending execution thereof in response to execution of a respective operation instance, the respective operation instance coinciding with one of the coordination points therein."

Accordingly, no *prima facie* case of obviousness has been made and claim 35 and those dependent therefrom (36-41) are **allowable** at least for this reason.

Furthermore, Applicants respectfully note that at least claims 35-37 and 39-41 find full support in U.S. Patent 6,308,319 to which the present application claims priority. The Office relies on *Rozas* (in addition to *Kawaguchi*) in its obviousness rejection. Since Applicants' priority antedates *Rozas*, the aforementioned claims are each **allowable** for at least this reason as well.

As before, the Office's reliance on Official Notice for the proposition that an unused position in an instruction sequence is typically a NOOP instruction is nonsensical as applied to Applicants' claim(s). Applicants do not recite a NOOP. For completeness, Applicants **dispute** and **demand** authority for the proposition as apparently applied in rejecting the claims.

Claim 36

No reference for *use of delay slots of delayed control transfer instructions* has been cited by the Office. Accordingly, there is no prima facie case of obviousness and claim 36 is **allowable** at least for this reason. *Rozas* does not precede Applicants' priority date. Claim 36 is allowable for this reason as well. Furthermore, to the extent that the Office relies on Official Notice (as taken in rejection of claim 3), Applicants **dispute** and **demand** authority as provided above.

Claims 37 and 38

To the extent that the Office relies on Official Notice (as taken in rejection of claim 3), Applicants **dispute** and **demand** authority as provided above.

Claim 39

No reference for *suspension triggering operations coinciding with synchronization points for thread state synchronization amongst plural threads of execution* has been cited by the Office. Accordingly, there is no *prima facie* case of obviousness and claim 39 is **allowable** at least for this reason. *Rozas* does not precede Applicants' priority date. Claim 39 is allowable for this reason as well. Furthermore, to the extent that the Office relies on Official Notice (as taken in rejection of claim 3), Applicants **dispute** and **demand** authority as provided above.

Claim 40

No reference for *suspension triggering operations coinciding with safe points at which plural threads have a consistent state* has been cited by the Office. Accordingly, there is no *prima facie* case of obviousness and claim 40 is **allowable** at least for this reason. *Rozas* does not precede Applicants' priority date. Claim 40 is allowable for this reason as well. Furthermore, to the extent that the Office relies on Official Notice (as taken in rejection of claim 3), Applicants **dispute** and **demand** authority as provided above.

Claim 41

No reference for:

safe points at which information descriptive of those temporary storage locations containing references to dynamically-allocated memory in the context of each function in a calling hierarchy of functions of a respective of the plural threads is ascertainable by a memory reclamation component for use in defining a root set of references to the dynamically-allocated memory

has been cited by the Office. Accordingly, there is no prima facie case of obviousness and claim 41 is **allowable** at least for this reason. *Rozas* does not precede Applicants' priority date. Claim

41 is allowable for this reason as well. Furthermore, to the extent that the Office relies on Official Notice (as taken in rejection of claim 3), Applicants **dispute** and **demand** authority as provided above.

Claims 42-46

Applicants respectfully request that the Office re-read the language of claim 42 which recites:

A method of coordinating garbage collection with execution of a multi-threaded mutator, wherein the garbage collection is performed at safe points in an execution trajectory of the multi-threaded mutator, and wherein potentially inconsistent threads of the multi-threaded mutator are suspended at the safe points to facilitate the garbage collection, the method comprising:

upon a start garbage collection event, encoding an exception triggering value in storage referenced by exception triggering instructions in otherwise unused operation slots of instruction encodings that coincide with the safe points;

thereafter, upon execution of the exception triggering instructions, suspending the corresponding one of the threads; and

performing the garbage collection after each of the threads is suspended.

Kawaguchi and *Rozas* have nothing to do with garbage collection. Indeed, the Office acknowledges same, but asserts that garbage collection is merely a specific example of an exception. This is not true. A garbage collection infrastructure (like many software constructs) may employ exceptions for triggering events; however garbage collection operations (as recited in the claim) are not simply "specific example[s] of an exception." Accordingly, Applicants, once again, **dispute** and **demand** authority for Examiner's factual assertion.

Furthermore, the assertion is entirely irrelevant. In essence, the Office's position appears to be that an otherwise novel, non-obvious mechanism that provides useful concrete and tangible

results is obvious because claimed subject matter is necessarily implemented using constructs that exist on a real processor and are therefore known. The Office's position is simply not consistent Federal Circuit law.

In any case, since

(1) no garbage collection (GC) start event,
(2) no encoding of an exception triggering value upon a GC start, and
(3) no encoding of an exception triggering value in an operation slot coinciding with a safe point ...;

have been cited by the Office, there is no prima facie case of obviousness and claim 42 (as well as claims 43-46 which depend therefrom) is **allowable** at least for this reason.

As before, *Rozas* does not precede Applicants' priority date. Claims 42-46 are allowable for this reason as well.

Finally, the Office's reliance on Official Notice for the proposition that an unused position in an instruction sequence is typically a NOOP instruction is nonsensical as applied. Applicants do not recite a NOOP. For completeness, Applicants **dispute** and **demand** authority for the proposition as apparently applied in rejecting the claims.

Claim 43-45

To the extent that the Office relies on Official Notice (as taken in rejection of claim 3 or claim 4), Applicants **dispute** and **demand** authority as provided above.

Claim 46

The Office cannot seriously suggest that *Kawaguchi's* tables (Figs. 13A-16) have anything to do with storage maps identifying storage locations reachable by a multi-threaded mutator at a safe point. *Kawaguchi's* tables encode permissions and exception handling directives.

Claims 47-52

Kawaguchi does not discloses or suggest a processor "having an instruction set that includes an exception triggering operation encodable in an operation position of an instruction encoding for parallel execution of component operations." *Rozas* does not precede Applicants' priority date and is therefore not a proper reference under any section of 35 U.S.C. § 102 (at least with respect to claims 47-50 and 52). Accordingly, claim 47 and those dependent therefrom are allowable.

Even if *Rozas* were a proper reference, there is simply no "teaching, suggestion or motivation" to introduce a VLIW instruction encoding into *Kawaguchi's* apparatus, which is fundamentally a single processor, single-execution unit architecture. Indeed, a VLIW instruction encoding would not be suitable for, or operative with, *Kawaguchi's* apparatus. The Office position appears to be that *Rozas* provides the suggestion to encode as VLIW instructions because it discloses VLIW instructions and schedule optimizations therefor. This is reasoning circular and factually incorrect. There is simply no factual basis to suggest that wholesale redesign of *Kawaguchi's* apparatus to introduce multiple execution units and VLIW instruction encodings is an optimization to address a disclosed or inherent limitation of *Kawaguchi's* apparatus. Once again, the Office employs Official Notice as a strategy to avoid its burdens under the law of obviousness. Applicants **dispute** and **demand** authority for the proposition as apparently applied in rejecting the claims.

In truth, the only "motivation" that the Examiner finds, is in the language of Applicants' claim, namely the phrase "instruction encoding for parallel execution" which is broad enough to encompass VLIW encodings (as well as other encodings, such a delay slot encodings). Use of Applicants' claim (or disclosure) as the required "teaching, suggestion or motivation" is clear legal error. Applicants respectfully request withdrawal of the rejections.

Art Rejection Under 35 U.S.C. §103, Kawaguchi, Rozas and Charnell

Claims 30-31 and 33 are rejected under 35 U.S.C. §103(a) as being unpatentable over *Kawaguchi* in view of *Rozas* and further in view of U.S. Publication 2002/0029357 A1 by Charnell et al. (hereinafter *Charnell*). Applicants respectfully traverse.

Because *Charnell* does not disclose the missing limitations, each claim is **allowable** at least for the reasons given above with respect to the claims from which they depend.

Furthermore, Applicants respectfully note that claims 30-31 and 33 find full support in U.S. Patent 6,308,319 to which the present application claims priority. The Office relies on *Charnell* (in its obviousness rejection) for a Just-In-Time (JIT) compiler. *Charnell* does not precede Applicants' priority date and is therefore not a proper reference under any section of 35 U.S.C. § 102 with respect to claims 30-31 and 33. Accordingly, claims 30-31 and 33 are **allowable** for at least this reason as well.

Finally, Applicants must (once again) **dispute** the Office's use of Official Notice ("Official Notice is taken that Kawaguchi's invention could have been modified to accommodate a JIT compiler, as they are well known in the art for receiving source code and encoding an operation (including any trap / exception) as encountered.") Really? How would that work? What aspect would be modified (given that no compilation, compiler or similar facility is described in *Kawaguchi*)? Again, the Office (in effect) makes a legal conclusion as to obviousness under the guise of "Official Notice." Applicants **dispute** and **demand** authority for the proposition as apparently applied in rejecting the claims.

CONCLUSION

In summary, claims 1-52 are in the case. All claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is respectfully solicited. Nonetheless, if any issues remain that could be more efficiently handled by telephone, the Examiner is requested to call the undersigned at the number listed below.

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that, on the date shown below, this correspondence is being

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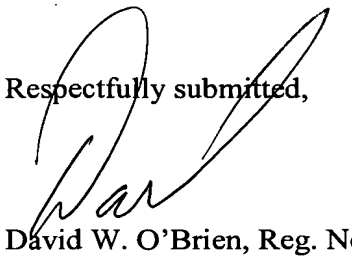
Respectfully submitted,



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AMENDMENTS TO THE DRAWINGS

The attached sheet of drawings include changes to Fig. 3 and replace the original sheet including such figure.

Attachment(s): Replacement Sheet including amended Fig. 3.